AMENDMENTS TO THE CLAIMS

The claims in this listing will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) An N-way set-associative cache memory, comprising:

a control register operable to indicate one or more ways among N ways;

a control unit operable to activate the way indicated by said control register; and

an updating unit operable to update contents of said control register,

wherein the control register is configured to dynamically set the activated way based on a process executed by a processor, and

wherein the control register prevents data from being evicted from the cache memory by other tasks after task switching, and inhibits influence of the other tasks on a hit ratio following the task switching.

2. (Currently Amended) The cache memory according to ~~Claim~~ claim 1,

wherein said control unit is operable to restrict at least replacement, for a way other than the active way indicated by said control register.

3. (Currently Amended) The cache memory according to ~~Claim~~ claim 1, further comprising:

a tag holding unit, provided for each of the ways, operable to hold, as a tag, a cache data address; and

N-comparison units operable to judge whether a hit or a mishit has occurred, by comparing a tag address and N-tags outputted by said tag holding unit, the tag address being an upper portion of a memory access address outputted from a processor,

wherein said control unit is operable to disable a comparison unit corresponding to a way other than the active way indicated by said control register.

4. (Currently Amended) The cache memory according to ~~Claim~~ claim 3,

wherein said control unit is operable to disable tag outputting to a comparison unit, for a cache address holding unit corresponding to the way other than the active way indicated by said control register.

5. (Currently Amended) The cache memory according to ~~Claim~~ claim 3,

wherein, when a memory access address is outputted from the processor, said control unit is operable to:

control said comparison units to perform, for a maximum of two times, tag comparison for the memory access address;

disable, in a first tag comparison, a comparison unit corresponding to the way other than the active way indicated by said control register; and

cause said comparison units to perform a second comparison, without disabling the comparison unit corresponding to the way other than the active way, in the case where it is judged that a mishit has occurred in the first tag comparison.

6. (Currently Amended) The cache memory according to ~~Claim~~ claim 5,

wherein said control unit is operable to disable, in the second tag comparison, the comparison unit corresponding to the way other than the active way.

7. (Currently Amended) The cache memory according to ~~Claim~~ claim 2,

wherein said control unit is operable to prohibit status updating for the way other than the active way indicated by said control register.

8. (Currently Amended) The cache memory according to ~~Claim~~ claim 2,

wherein said control unit is operable to prohibit updating of information indicating an access order of the way other than the active way indicated by said control register.

9. (Currently Amended) The cache memory according to ~~Claim~~ claim 2, further comprising

a reset unit operable to reset the information indicating an access order for the ways, when the contents of said control register are updated by said updating unit.

10. (Currently Amended) The cache memory according to ~~Claim~~ claim 9,

wherein the information indicating the access order is 1-bit data for each cache entry,

said cache memory further comprises

a register operable to hold data indicating a round position for selecting, in a round robin, one way from a plurality of replaceable ways, and

said reset unit is operable to reset said register when the contents of said control register are updated by said updating unit.

11. (Currently Amended) The cache memory according to ~~Claim~~ claim 2,

wherein said updating unit includes:

a holding unit operable to hold way data for respective tasks, which specifies a way to be activated; and

a rewriting unit operable to rewrite said control register so as to hold way data corresponding to a task being executed.

12. (Currently Amended) The cache memory according to ~~Claim~~ claim 11,

wherein said holding unit is operable to hold the way data as part of context data for the respective tasks which is stored in a memory, and

during task switching, said rewriting unit is operable to save, in the memory, way data of a current task, inside said register, and to restore, from the memory to said control register, way data of a next task.

13. (Currently Amended) The cache memory according to ~~Claim~~ claim 12,

wherein said holding unit is operable to hold the way data for the respective tasks, and

said rewriting unit includes:

an address storage unit operable to store an address range of the respective tasks, stored in the memory;

an identification unit operable to identify the task being executed, based on the address range stored in the address storage unit and an instruction fetch address outputted from a processor; and

a selection unit operable to select, from said holding unit, way data corresponding to the identified task being executed.

14. (Currently Amended) The cache memory according to ~~Claim~~ claim 12,

wherein said holding unit is operable to hold the way data for the respective tasks,

said rewriting unit includes:

a selection unit operable to select way data from said holding, according to a task number outputted from a processor unit, the way data corresponding to a task being executed; and

a writing unit operable to write the selected way data into said control register.

15. (Currently Amended) The cache memory according to ~~Claim~~ claim 11,

wherein way data held in said holding unit is assigned to a task, by an operating system.

16. (Currently Amended) The cache memory according to ~~Claim~~ claim 1,

wherein a unit of replacement for respective ways can be switched between a line size of a cache entry and a size which is one over two to the nth power of the line size,

said control register is further operable to indicate a replacement size for respective tasks, and

said control unit is operable to perform replacement control with the replacement size indicated by said control unit.

17. (Currently Amended) The cache memory according to ~~Claim~~ claim 16,

wherein said control unit is operable to restrict at least replacement for a way other than the active way indicated by said control register, and to perform replacement on the active way indicated by said register, with the size indicated by said control register.

18. (Currently Amended) The cache memory according to ~~Claim~~ claim 17,

wherein said updating unit includes:

a holding unit operable to hold way data for respective tasks, specifying a way to be activated, and the replacement size for the respective tasks; and

a rewriting unit operable to rewrite said control register so as to hold way data and a replacement size corresponding to a task being executed.

19. (Currently Amended) The cache memory according to ~~Claim~~ claim 1, further comprising:

a storage unit operable to store, for each cache entry, 1-bit access information indicating whether or not the cache entry has been accessed, the cache entry holding data which is a unit of caching; and

a selection unit operable to select a cache entry to be replaced from among cache entries corresponding to access information indicating that a cache entry has not been accessed.

20. (Currently Amended) The cache memory according to ~~Claim~~ claim 19, further comprising:

a register operable to hold data indicating a round position for selecting, in a round robin, one way from a plurality of ways that can be replaced; and

a reset unit operable to reset, when the contents of said control register are updated by said updating unit, information indicating an access order for ways, and the data, in said register, indicating the round position.

21. (Currently Amended) A control method for controlling an N-way set-associative cache memory, comprising:

~~a step of~~ setting, to a control register, way data indicating one or more ways among N ways; and

~~a control step of~~ activating the way indicated by the control register,

wherein the control register is configured to dynamically set the activated way based on a process being executed by a processor; and

wherein the control register prevents data from being evicted from the cache memory by other tasks after task switching, and inhibits influence of the other tasks on hit ratio following task switching.

22. (Currently Amended) The control method according to ~~Claim~~ claim 21,

wherein in said controlling, at least replacement is restricted for a way other than the active way indicated by the control register.

23. (Currently Amended) The control method according to ~~Claim~~ claim 22, further comprising an updating step of reading-out, from a holding unit, way data corresponding to a task being executed, and writing the read-out way data into the control register, the holding unit holding way data for respective tasks, the way data specifying a way to be activated.